REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants wish to thank the Examiner for the notice that claim 20 has been allowed.

Applicants attorney wishes to thank Examiner Kim for the courtesies extended during the telephone conference of May 5, 2004. In response to the conversation, Applicants have amended claims 2, 8 and 13 which is believed to be an inherent limitation that was already present in these claims, which indicates that the engine clock source is a different clock signal for example that provides an output clock different from the memory clock source. As such both an engine clock source and memory clock source are claimed along with, for example, the switching circuit and memory clock tree circuit as claimed (see claim 2).

Applicants have also added new claims 21-26 as depending from allowable claim 20. As such, these claims are also believed to be in condition for allowance and since they add additional novel and non-obvious subject matter.

Claims 1, 4 and 7 stand rejected under 35 U.S.C. §102 (e) as being anticipated by Linn.

With respect to Claim 1, Lin fails to disclose a power consumption reduction circuit comprising a memory clock source of a graphic controller; and a memory clock tree circuit of a graphics controller, operatively coupled to the memory clock source, that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode. Lin is dedicated to a compiler system and discloses a system requiring a compiler and method whereby *compiled machine code instructions* from a compiler indicate

which functional unit on a single microelectronic device are to be turned on or off. (Emphasis added). In response to machine code instructions, a logic unit provides a *system clock signal* on the appropriate clock input line for the functional unit that is to be turned on. (Emphasis Added).

Applicants respectfully submit that the system clock source and monitoring information from machine code instructions as taught by Lin are not analogous to a memory clock source of a graphics controller and received condition data as taught by Applicants. In reference to Applicants' Figure 3, a memory clock source is operatively coupled to a memory clock tree circuit that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for different processing engines. *In response to received condition data*, the memory clock tree circuit selectively activates at least some of the plurality of independent clock signals. (Emphasis added). Independent clock signals selectively activated by the memory clock tree circuit are provided to a corresponding plurality of corresponding individual buffer circuits and memory request interfaces. As illustrated in Figure 3, the plurality of corresponding memory request interfaces activated by independent clock signals request data from a memory controller (Element 310). As such, the memory controller may utilize a power consumption reduction circuit as illustrated in Figure 2 to accept a memory read request signal and provide latched memory read data. In addition, an engine clock circuit (Fig. 3, Element 306) provides a *separate and distinct engine clock* signal to a plurality of requesters and engine blocks corresponding to memory request interfaces activated by the memory clock tree circuit. (Emphasis added).

In contrast to Applicants' memory clock source, a *system clock* (Fig. 4, Element 104) of Lin is directly provided to the plurality of functional units based on a compiler and *compiled machine code instructions*. (Emphasis added). The functional units provided with the system

clock signal are operatively turned on for the duration of the system clock signal. Applicants' claimed invention is not responsive to compiled machine code instructions in the form of monitoring information, as taught by Lin; rather, the Applicants' claimed invention receives *condition data* during an active mode. (Emphasis added). Applicants' claimed invention operates using a memory clock and requires a memory clock tree circuit of a graphics controller. When read in light of the Specification, condition data may include, inter alia, data indicating that a primary or secondary display has been selected, data indicating a graphic user interface engine is active, data indicating that video overlay scaler has been enabled, data indicating whether said picture operations have been enabled, and data indicating a video capture operation has been enabled. (Page 5, Lines 25-28). In summary, Lin discloses a compiler based system that uses a compiler to receive source code and compile to machine code instructions, and does not control a memory clock based on received condition data.

In light of above remarks, Applicants respectfully note that Lin fails to teach or disclose the limitations expressed in Applicants' claim 1. Applicants respectfully believe claim 1 is in proper condition for allowance.

With respect to claim 4, the Applicants respectfully repeat the relevant remarks made in regard to claim 1, and further submit that claim 4 contains further patentable material. While Lin discloses a logic unit (FIG. 5, Element 116) and a plurality of latch circuits (FIG 5, Elements 504, 510, 516 and 522), Lin merely teaches an alternative approach for turning on and off the functional units. By not allowing the inputs of functional units to change state, a plurality of latches hold the previous inputs based upon control lines generated by a logic unit responsive to monitoring information from machine code instructions. (Col. 10, Lines 5-17). In contrast, the Applicants' Specification teaches a separate structure in which a plurality of *memory read*

latches are dynamically activated and deactivated based on detected memory read requests to facilitate memory access activity based power reduction. (Emphasis Added). Specifically the memory read latch control circuit includes a read data latency compensation circuit which determines how long it takes for the memory to fetch data. The memory read latch control circuit includes control logic that receives the memory read request, obtains the read data latency information and generates a read latch control signal which indicates when to turn off the read latching flops during an active mode to reduce power consumption. The memory read latch control circuit also includes an AND circuit responsive to the read latch control signal and also responsive to a memory clock signal generated by the memory clock source. The AND circuit selectively enables and disables the memory read latches by generating the enable signal as a function of the memory request. (Figure 2, Element 204; Page 6, Line 27-Page 7, Line 19). In addition, the Applicants teach a plurality of memory read latch circuits which receive memory data and are responsive to the memory read latch control circuit. As Lin fails to disclose the limitations of memory read latches and corresponding circuitry as set forth in claim 4, the Applicants respectfully believe that claim 4 is in proper condition for allowance.

With respect to claim 7, the Applicants respectfully repeat the relevant remarks made above. In failing to disclose a power consumption reduction circuit comprising a memory clock tree circuit that selectively activates at least some of a plurality of independent clock signals in response to *receive condition data*, Lin also fails to disclose the subsequent claim limitations. In light of the above remarks, the Applicants respectfully believe that claim 7 is in proper condition for allowance.

Claims 2 and 17-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin. The Examiner has cited the system clock and logic unit (Figure 4, Elements 104 and 116,

respectively) as teaching an engine clock source operatively coupled to a switching circuit that generates an output clock signal. The Applicants are confused to the Examiner's rejection of claim 2 as the Examiner also cited the system clock of claim 4 against the memory clock source of Applicants' claim 1. The Applicants respectfully note that two clock sources, a memory clock source and a distinct engine clock source, are taught in Applicants' claimed invention. In contrast, the Lin reference only discloses one clock, namely a system clock. As such, the Lin reference fails to disclose not only the memory clock source of Applicants' claim 1, but also an engine clock.

Moreover, the inclusion of a video overlay engine, a video capture engine, an I2C control logic, a multimedia port, and video capture enable data in a power consumption reduction circuit such that the switching circuit disables the output clock signal based on condition data as listed in claim 2 further distinguishes the Applicants' claimed invention from that of Lin. For example, Lin discloses a compiler-based system and is not directed to a graphics controller or video controller as taught in Applicants' claims 1-2. Applicants respectfully request a showing of factual basis for the alleged motivation to include at least one of: video overlay engine, a video capture engine, an I2C control logic, a multimedia port, and video capture enable data in a power consumption reduction circuit. Furthermore, Applicants request the exact teaching that shows that such devices are "well known in the art of computer system[s]." (Office Action, Page 4, ¶ 12). Such a combination of devices included in the limitations of Applicants' claim 2 with Lin would nevertheless result in a compiler-based video capture system not disclosed by Lin or other references or claimed by Applicants. Moreover, as claim 2 inherits the limitations of claim 1, Applicants respectfully believe claim 2 is in proper condition for allowance.

With respect to claims 17-19, the Applicants respectfully repeat the relevant remarks made above in regards to claim 1. Specifically, the Lin reference fails to disclose the activation of a plurality of independent clock signals in response to *received condition data* during an active mode. As a result, the Lin reference furthermore fails to disclose any limitations upon said condition data. Claims 17-19 are respectively believed to be in proper condition for allowance.

New claim 27 is effectively the combination of claims 1, 3 and 4. This claim is also allowable since the references do not appear to teach, alone or in combination, among other things, a memory clock source of a graphics controller and an associated memory clock tree circuit and branches of memory clocks and memory interface circuits for differing processing engines while varying the speed of memory clocks based on the type of memory request in combination with memory read latch circuits and memory read latch control circuits as claimed.

Applicants respectfully submits that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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